# A NOVEL INTEGRATED MICROWAVE BIAS NETWORK FOR LOW COST MULTISTAGE AMPLIFIERS

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## ABSTRACT

A novel MMIC bias network topology utilizing FETs has been developed. The bias network is very compact, providing low DC path loss with high, broad band RF isolation. This bias network consists of two FETs and a capacitor, and is implemented in pseudomorphic HEMT. The bias network is useful in multi-stage amplifiers where stage-to- stage RF isolation is critical to system stability and performance. A VGA (Variable gain amplifier) is shown with measured results as a application example of the bias network. There is no other known published information or patents on this bias network topology.

## INTRODUCTION

In modern MMICs (Monolithic Microwave Integrated Circuit) in order to operate at low voltages one must operate multiple stages from a common DC source. However, implementing such a bias network for an integrated circuit that operates at microwave frequencies is difficult from both a financially viable (semiconductor real estate) and electrically stability (good RF isolation) point of view. The bias network [1] described in this paper and shown in Figure 1 demonstrates excellent DC and RF performance while occupying minimal semiconductor real estate.

## BACKGROUND

When DC biasing a multi-stage FET amplifier, RF and microwave signal leakage through the bias system can cause instability and reduction in gain. Traditional multi-stage RF and microwave amplifier systems use a separate drain bias supply with appropriate choking and filtering for each amplifier stage. Such a circuit is shown in Figure 2. This circuit is common among hybrid and monolithic circuits. This circuit requires separate bond pads and more complex packaging making it generally too costly, despite good DC and RF performance.

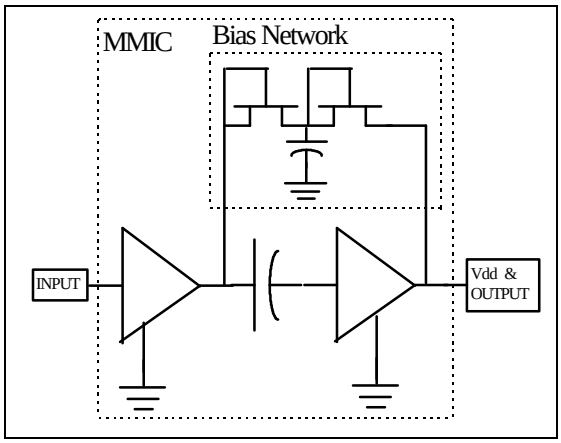


***Figure 1. Monolithic bias circuit for mulit-stage RF and microwave amplifiers*.[1]**

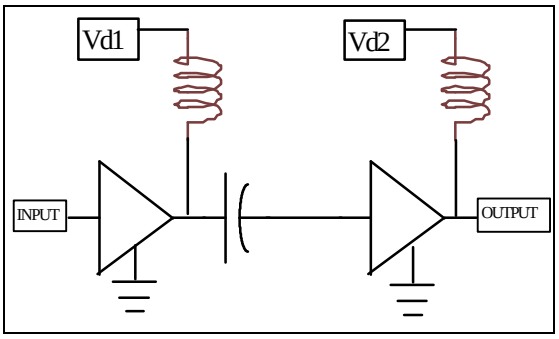


***Figure 2. Traditional bias network for multistage amplifiers*.**

Figure 3 shows three common approaches to this problem. Figure 3a shows the common approach of using an inductor to high-pass filter the RF and microwave signal. Unfortunately, even large inductors have limited bandwidth and require a large amount of semiconductor real estate. This inductor can also resonate, causing unforseen instability. Figure 3b shows that a single current source can be used. However, this circuit suffers from poor high frequency isolation since the signal will eventually capacitively couple across the FET. The last bias network [9] is shown in Figure 3c. It provides

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excellent broad band performance, but requires the current to be shared between stages, limiting operation to systems where sufficient voltage is available.

## THE RF AND MICROWAVE BIAS NETWORK

The bias network, as shown in Figure 1, is an evolution from the previous bias networks. It is implemented with two current sources and a capacitor. The use of the current source provides the low DC resistance while still presenting a high RF impedance. By using two current sources, the two ends of the network are further electrically isolated from each other. The use of the capacitor between the current sources is the key to high frequency performance. Since a current source provides a high RF impedance to the DC line, even a small amount of parasitic capacitance across the current source can lead to a severe degradation in isolation at RF to microwave frequencies.

The current sources are commonly implemented utilizing depletion mode FETs and connecting the gate and source together. The capacitor is normally implemented with a dielectric between two metal layers. The FETs and capacitor can be small, so implementation of this bias network can be achieved in very little semiconductor area. Once both FETs are brought into a saturated range of the I-V curve, very little additional DC resistance is seen. The effective voltage drop across the bias network is approximately 0.8V, over a wide range of DC currents. Figure 4(a) shows the equivalent DC structure. Selection of the FET size determines the current handling capability of the bias network.

RF and microwave signals are trapped in the linear range of the I-V curve. The high frequency signal encounters a great deal of series resistance. However, parasitic capacitance can allow the signal to couple across because of the high FET impedance. The bias capacitor effectively lowers the impedance between the FETs and provides low-pass filtering. The bias capacitor is carefully selected to fully compensate for the parasitic FET capacitance. Figure 4(b) shows the equivalent RF structure

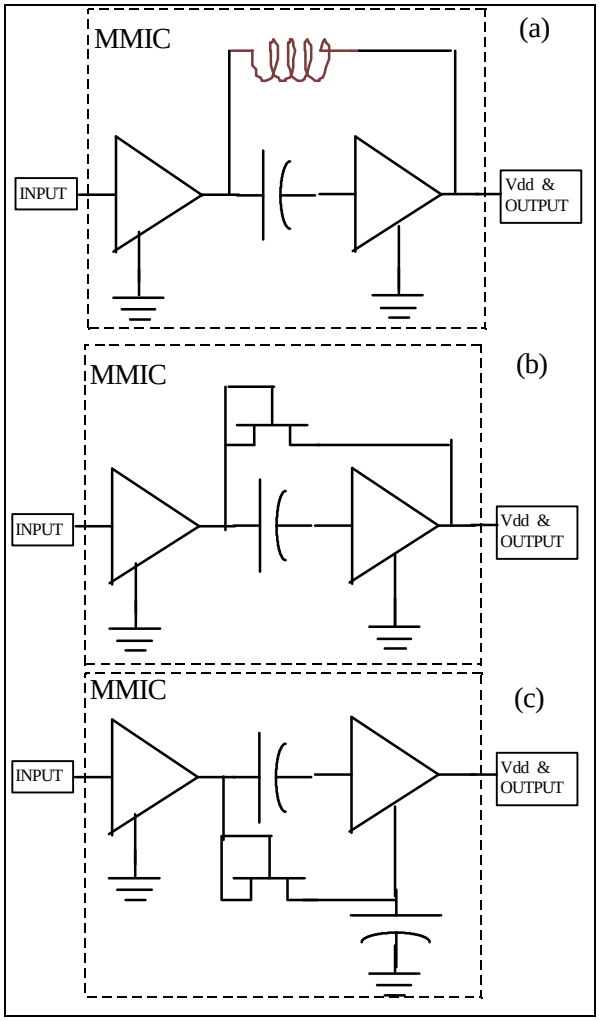


***Figure 3. Common MMIC bias networks.***

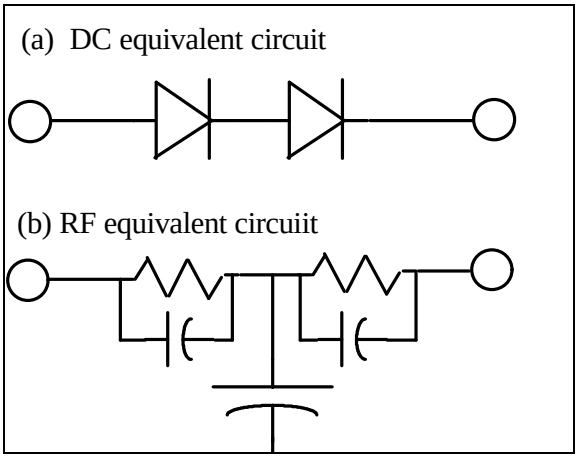


***Figure 4. DC and RF equivalent topologies for the bias network.***

## DESIGN EXAMPLE

A VGA (Variable Gain Amplifier) design was fabricated and built, demonstrating the effectiveness of the bias network. The VGA topology in this case required a very high isolation bias network in order to ensure it had sufficient isolation at the maximum attenuation state. The VGA is often used on the transmit section of a wireless receiver in a AGC (Automatic Gain Control) section to properly set and maintain the gain and output power. Increasingly, modern digital wireless systems employ VGAs on the receive side to increase linearity and to "de-sensitize" the mobile system from the cell antenna location.

The devices used in this monolithic design were pseudomorphic high electron mobility transistor (PHEMT) structures built using molecular beam epotaxy (MBE) material growth techniques. The gates were defined using electron-beam lithography. Gate lengths range from 0.12 to 0.17 microns. The remaining layers are placed on the 3-inch wafers using precision steppers. The result is a process with typical $F_T$ of 60 GHz and able to operate utilizing very low voltage and current density

This high frequency VGA is designed to give the range and performance of a traditional VGAs that use "bias-down" dual gates or diodes. The main drawback to this "bias-down" technique is that both I/O match and linearity change significantly over the attenuation range, degrading functionality. This VGA utilizes the bias network and multiple stages to maintain constant input and output match and give a wide attenuation range. As Figure 5 shows, a three stage design is used. The first stage sets the input match, some gain, and noise figure. The second stage is a basic voltage controlled attenuator. The third stage sets the remaining gain, output match, and output power.

The topology for the VGA, shown in Figure 6, was selected for it's integrated compactness as well as it's performance. The first stage consists of a heavily fedback common source FET with an integrated source bypass capacitor and bias setting current source. The second stage consists of two FETs in series configured with zero drain-to-source voltage so that they are essentially voltage controlled resistors. DC blocking capacitors and a voltage divider are employed to allow the drain/source voltage to be set to 2V from a 3V supply. This allows the control voltage for maximum attenuation be set at 1V (-1V gate-to-source), well beyond the -0.5V PHEMT FET pinch-off voltage. The last stage is again a heavily fedback common source FET utilizing an external source capacitor and integrated current source.

This paper will not delve into the exact values for all capacitors, FETs, and resistors. It will suffice to focus on the bias network. The total current goal for the MMIC was 16 mA, with first stage allocated 7 mA. Two, 75 micron, current sources were selected to form the active core of the bias network. These provided enough RF impedance while keeping the total voltage drop across the network to about 1.2 V. A 1.0 pF capacitor was selected for the bias network since it was the best compromise between size (250 sq. microns) and isolation (25 dB).

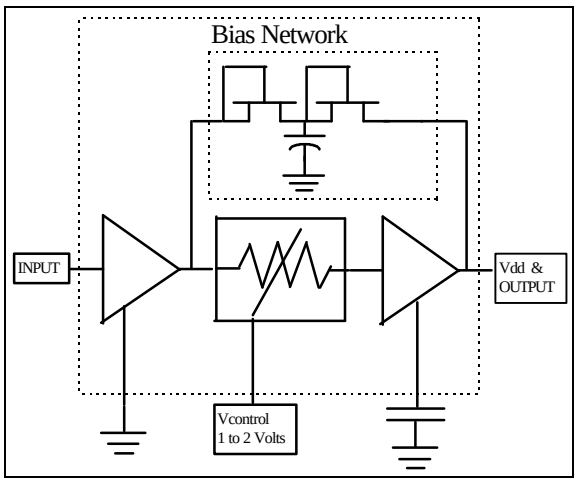


***Figure 5. Block representation of the PHEMT VGA***

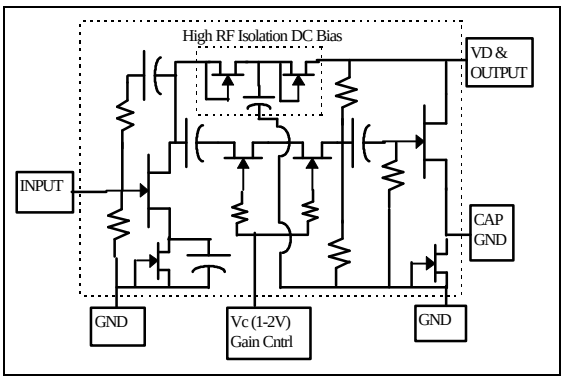


***Figure 6. PHEMT MMIC VGA Schematic***

Realization of the VGA is shown in figure 8. The die measured only 0.45mm by 0.45 mm. Measured on-wafer performance shows over 20 dB of gain control from 0.8 Ghz to 6.0 Ghz. Figure 7 shows the typical maximum gain is +10 dB with +2V applied to the control line Vc. Typical maximum attenuation is -10 dB with +1V control and poor below 2 Ghz due to limitations of the test system. Packaged measurements have shown at least 10 dB average attenuation down to 500 MHz.

The novel bias network used in the VGA provided in excess of 30 dB isolation across the prescribed 0.8 to 6.0 Ghz bandwidth. The 30 dB is derived from the 20 dB VGA maximum attenuation plus the extra 10 dB gain that the first stage provided. Other design examples built using traditional inductors or single current source bias network were only able to provide 15 to 20 dB of isolation through the network.

A novel integrated microwave bias network for muilti-stage amplifiers has been developed and performance demonstrated. This bias network is extremely useful in applications where DC power needs to be distributed to multiple stages but high RF signal isolation needs to be maintained. The bias network is compact and easily integrated. Patents have been filed on the behalf of Hewlett-Packard in regards to its use. A variable gain amplifier has been shown to demonstrate the effectiveness of the bias network. The multistage VGA fulfilled it's attenuation range and I/O match goals through the use of the bias network. Performance data has been shown. Special thanks is given to Chris Pease, Carlos Mendoza, Tuan Lam, Bob Myers, John Coward, Jeff Raggio, Vince Du, and Craig Snapp for their help and support in this project.

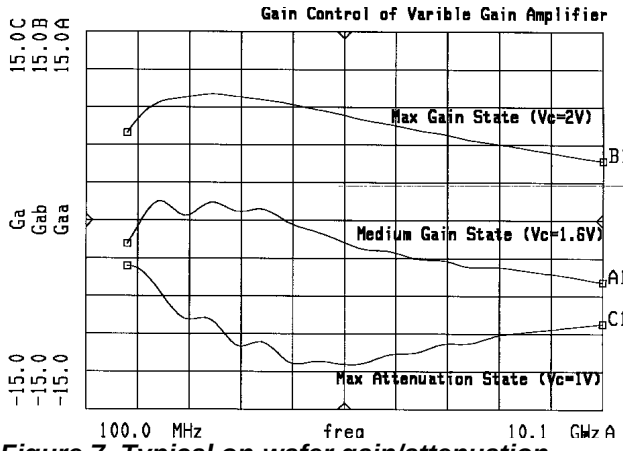


***Figure 7. Typical on-wafer gain/attenuation***

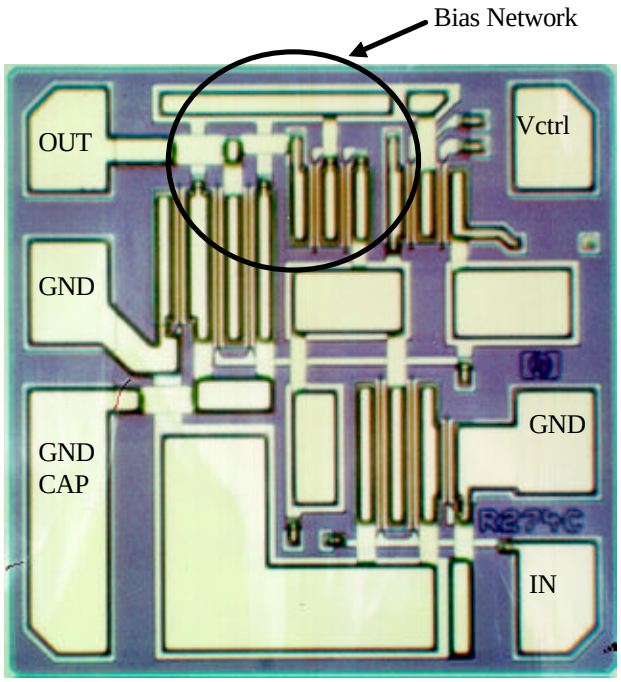


***Figure 8. Photograph of MMIC as fabricated.***

## REFERENCES


1. H. Morkner, M. Frank, K. Negus, "A Bias Network For Multi-Stage Amplifiers", 5 Claims, Filed at U.S. Patent Office, Oct 1996
2. H. Morkner, C. Siu, B. Myers, "Designing Miniature GaAs and Silicon Building Blocks", *Wireless Design and Development*, Sept. 1996, pp 17-20.
3. H. Morkner, "Miniature 3V GaAs LNA, VGA, and PA for Low Cost .5-4 Ghz Wireless Applications", *1996 Wireless Symposium,* Feb 1996.
4. H. Morkner, N. Nguyen, A, Ward, B. Myers, G. Carr, "Design and Utilization of Wireless Monolithic Low Noise Amplifiers fot 3 Volt, Low Current Applications", *1995 RF Expo West*, Jan 1995.
5. H. Morkner, N. Nguyen, G. Carr, "Monolithic Gain Blocks in Mini-Packages for DC to 4000 MHz Wireless Hand-Held Communication", *1995 Wireless Symposium,* Feb 1995.
6. M. Williams, F. Bonn, C. Gong, T. Quach, "GaAs RF ICs Target 2.4-GHz Frequency Band", *Microwaves and RF*, July 1994, pp 111-118.
7. H. Morkner, M. Frank, D. Millicker, "A High Performance 1.5 dB Low Noise PHEMT MMIC Amplifier for low cost 1.5 - 8 GHz Commercial Applications", *1993 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp 13 - 16.
8. H. Morkner, M. Frank, R. Kishimura, "A Novel MMIC PHEMT Low Noise Amplifier for GPS Applications", *1992 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp 13-16.
9. P.M. Smith, P.C. Chao, K. Duh, L.F. Lester, B.R.Lee, and J.M. Ballingall, "Advances in HEMT Technology and Applications", *1987 IEEE MTT-S International Symposium*, p. 749.
10. M. Frank, "The Current Source as a Microwave Biasing Element", US Patent # 4,912,430.
11. M. Frank, "The 2 to 6 GHz Block GaAs MMIC Amplifier", *Microwave Journal*, Aug. 1990, pp 83-92.